

## FIELD PROGRAMMABLE PROCESSOR 5

### FPP525 / FPP525E



#### OVERVIEW

The Field Programmable Processor 5 (FPP525 / FPP525e) represents the latest and highest performance real-time programmable processor line for the Base 550 and Avalon front-end telemetry acquisition and processing systems. The FPP5 enables the L-3 VME systems to achieve their industry-leading computational performance, now rated at over 4.85 million basic algorithms per second.

#### PERFORMANCE

The FPP5 dramatically enhances the system's algorithm processing and decommutation capabilities over software-based solutions. The FPP5 increases the performance of basic algorithms such as "average over n" and "fifth order EU conversions", and also boosts the performance of large gain algorithms used in signal analysis, secondary PCM decommutation, and other applications. Latest FPP5 improvements include support for up to 1 million tags for parameter processing under Vista 4.0 and enhanced algorithmic computational performance with the FPP525e.

For data distribution, the FPP5 achieves unprecedented performance in data transfer rates of over 4.5 million samples per second to Ethernet clients. The Gigabit Ethernet port on the FPP5 coupled with dramatic software optimizations enables this high throughput.

#### APPLICATIONS

Two MUXbus mezzanines can be added to the FPP5 for CDSI and CVSD applications. Alternatively, the SBC also supports 2 standard PMC slots for Fiber Channel and SCRAMNet applications. For maximum flexibility, algorithms from L-3's extensive libraries can be modified to create, simulate, test, and debug algorithms in the 'C' programming language on the system's workstations.

Data gather connections are established directly from the FPP5 to the client -- bypassing the System Controller module -- allowing data gather outputs to scale nearly as linearly as processing performance (2 FPPs mean twice the data throughput), up to the maximum incoming data rate of the receiving computers. Adding FPPs achieves a linear increase in system performance due to the system's parallel processing data flow architecture.

#### TECHNOLOGY

FPP5 uses a standard off-the-shelf 1 GHz PowerPC 6U VME single board computer (SBC) from Motorola, providing a ready upgrade path to emerging technologies. The SBC is connected to the system's high-speed processing bus, the MUXbus, via a 3U interface module.

#### KEY FEATURES

- Supports up to 1M tag addresses for parameter processing under Vista 4.0
- Processes 16- and 32-bit words directly including prime (raw) and derived (processed) data
- Performs nth-order EU conversions and secondary IRIG Class II PCM telemetry decommutation for complex multi-format embedded IRIG 1553 and asynchronous streams
- Uses C language for developing application-specific algorithms
- Utilizes COTS high performance PowerPC VME single board computers (SBCs)
- Links multiple standard and/or user-developed algorithms to form a large single algorithm chain
- Use multiple FPPs to achieve linear scalable increases in throughput for processing and data gathers
- Augment processing or I/O on the MUXbus with a variety of optional VME and PMC mezzanine modules

*Excellence You Can Measure*



## FIELD PROGRAMMABLE PROCESSOR 5

### FPP525 / FPP525E SPECIFICATIONS

#### Inputs

- MUXbus Data .....16- or 32-bit data input; prime (raw), derived, processed data from all input sources
- Maximum Parameters .....Up to 1M, dependent on number and type of algorithms per parameter and software version
- Input Formats .....32-bit binary, 2's complement, 1's complement, sign magnitude, offset binary, 32-bit exponential (IEEE 754-1985 floating point format)
- Interrupt .....VMEbus and MUXbus
- VME Interrupt .....Level 1 to 7, 32-bit vector

#### Processing

- Processor .....1 GHz 32-bit PowerPC 7455
- Memory:
  - Main Memory .....512 MB SDRAM
  - Cache .....2 MB L3 cache, 256 KB L2 cache
  - NVRAM .....32 KB total; 4 KB user
  - Battery .....5-year removable
  - EEPROM .....8 MB, 32 MB surface-mount
  - Input FIFO .....4K words
  - Output FIFO .....4K words
- Algorithm Library .....Over 150 algorithms included (e.g., nth-order polynomial, arithmetic, logical, compression)
- Embedded Decommuration
  - IRIG 106 .....PCM Class II asynchronous embedded decommuration formats; Chapter 8 MIL-STD-1553
- 100% acquisition standard
- Max. Throughput Rate .....4.85 million parameters

#### Algorithm Performance (nominal)

Algorithm	FPP4	FPP5	FPP5 Enhanced
1st-Order Polynomial	2.55 M / sec	3.84 M / sec	4.85M / sec
5th-Order Polynomial	2.15 M / sec	3.84 M / sec	4.85M / sec
Average Over n	3.54 M / sec	3.80 M / sec	4.85M / sec
In Limits	2.71 M / sec	3.68 M / sec	4.85M / sec
Bit Mask	2.76 M / sec	3.68 M / sec	4.85M / sec
96k All Long Gather		3.20 M / sec	4.50M / sec
Software Compatibility	FPP4	FPP5	FPP5 Enhanced
VISTA (min. version)	3.0	3.0	4.0
SWA500 (min version)	7.2	8.0	

#### I/O Options

- Ethernet .....2 ports (10/100/1000 Mbps, 10/100 Mbps)
- RS-232 .....1 port
- PMC Mezzanine .....2 modules
- MUXbus Mezzanine .....1 module
- MUXbus .....32-bit, 16-bit extended, or 16-bit zero extended integers, or 32-bit floating point for output, display, or further processing

#### Outputs

- Max. Number of Output Parameters per Module .....Up to 1M, tag address space for 65,535 parameters dependent on number and type of algorithms per parameter and software version

#### Functions

- Real-Time Derived Processing .....Single or linked; serial or in parallel on multiple processors
- Alarm Gathering .....Routed to MUXbus and/or graphics workstation for display
- Data Gathering .....Transfer selected real-time MUXbus data to the VMEbus

#### Program Setup and Control

- Keyboard and Mouse .....Fill-in-the-blank GUI displays with list-pick selections
- ASCII Text File .....User-created description
- API .....Application Programming Interface for remote setup (option)

#### General Requirements

- System 550/Avalon Chassis .....1 9U slot
- Maximum per Chassis .....14 (550) / 4 (Avalon)
- Maximum per System .....112
- Rear Panel .....RS-232 (RJ45 and DB25), Ethernet (RJ45) .....1 slot
- Power .....5V @ 8.0 A (typical)
- Environment .....See Base 550 System Chassis (PR0550A, PR0550B) and Avalon System Chassis (AVALON-R) data sheets
- Dimensions .....365mm (9U) x 160mm (Eurocard std.)
- Status Display .....8 LEDs and 8 character display

#### Compatibility

- Base 550 System Chassis (PR0550A, PR0550B)
- Avalon System Chassis (AVALON-R)
- SWA500 Applications Software
- VISTA Software

#### Ordering Information

- FPP525 .....Field Programmable Processor (FPP5)
- FPP525-CVSD .....Field Programmable Processor (FPP5) with CVSD Mezzanine
- FPP525-SCRM .....Field Programmable Processor (FPP5) with SCRAMNet Mezzanine
- FPP525-CDSI .....Field Programmable Processor (FPP5) with CDSI Mezzanine
- FPP525e .....Field Programmable Processor (FPP5), Enhanced Performance

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